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**TITLE: Apparatus and method for efficient sharing of
virtual
memory translations**

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Brief Summary Text - BSTX (18):

**FIG. 5 illustrates a TLB 60 corresponding to the operations
shown in FIG. 4.**

**Each TLB translation entry 62 (each row of the TLB 60) includes a
context**

**identification (CTX), a virtual address (VA), a physical page (PP),
and**

**attributes, such as a valid bit and protection bits. Note that the
physical**

**page (physical memory page address) PP.sub.-- X appears three
times in the TLB**

34. That is, (CTX.sub.-- i, VA.sub.-- i), (CTX.sub.-- j, VA.sub.-- j), and

**(CTX.sub.-- k, VA.sub.-- k) each map to the same physical page
PP.sub.-- X. It
would be highly desirable to provide a TLB that used a single TLB
entry for
every virtual address that maps to the same physical page. Such a
TLB would
greatly expand the information content possessed by a single TLB,
since a
single entry in the TLB could be used to map multiple virtual
addresses.**